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High speed ribbon optical link for the level 0 muon trigger

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Abstract

In this note we present the design of a high speed optical link which are foreseen to transfer data required by LHCb muon trigger. It is based on ribbon optical link and includes components to reduce the jitter of the TTC clock. We also describe the prototype board used to test and characterize such ribbon optical link. We measure a bit error rate below 10^{-15} at 1.6 Gbit/s. It is rather insensitive to the noise of the power supplies and the jitter of the input clock. The effect of single event upsets was estimated on the part of the ribbon optical link which will be implemented in the muon front-end electronics. We obtained an equivalent bit error rate of 3×10^{-11} in the radiation environment of the muon detector.

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1. Introduction

The principles retained in the muon trigger to transport the information from the Off Detector Electronics (ODE) to the processing board is based on 3 concepts :

- Serialization of the binary detector data ;
- Use of optical links as transport media ;
- Use of high integration optical devices.

Serial transmission reduces the number of signal lines and ground lines required to transmit data from one point to another. It also offers a high level of integration. We transmit 768 signals per board every 25 ns with only 24 serial links.

Using optical devices for high speed data transfer has a lot of advantages :

- High reliability for data transfer over 100 meters and more ;
- Complete electrical isolation avoiding ground loops and common mode problems.

In addition, the integration of several high speed optical links in a single device increases data rate while keeping the component count manageable and maintains a reasonable cost.

Parallel optical links integrate several optical transmitters in one module, several fiber connectors in one fiber connector and several optical receivers in one receiver module. The important benefit of parallel optical links is based on low-cost array integration of electronic and opto-electronic components. It also provides a low power consumption and a high level of integration.

In this note, we describe the parallel optical link foreseen to transfer data between the muon detector front-end and the level 0 muon trigger. In section 3, we demonstrate that the chosen devices allow high speed data transfers with a very low bit error rate. In section 4, we present the clock jitter filtering system designed to make the TTC clock compatible with high speed link requirements. In section 5 and 6, we describe the prototype board designed to characterize our high speed optical link and experimental results obtained with this test bench. Finally, we provide measurements of radiation effects which is largely dominated by single event upsets in the muon environment. We essentially measured the single event upsets sensitivity for most devices[1] involved in the emission chain since the emitter side of the link is close to the muon detector.

1 The ribbon optical transmitter was not tested due to a power supply failure. In this note, the effect of single event upsets on the transmitter is estimated from measurements made on a single optical transmitter.

2. High speed Ribbon Optical Link

The basic element for data transfer between the off detector electronic and the level 0 muon trigger is the parallel optical link containing 12 channels running at 1.6 Gbit / s. Figure 1 shows the organization of this optical ribbon link.

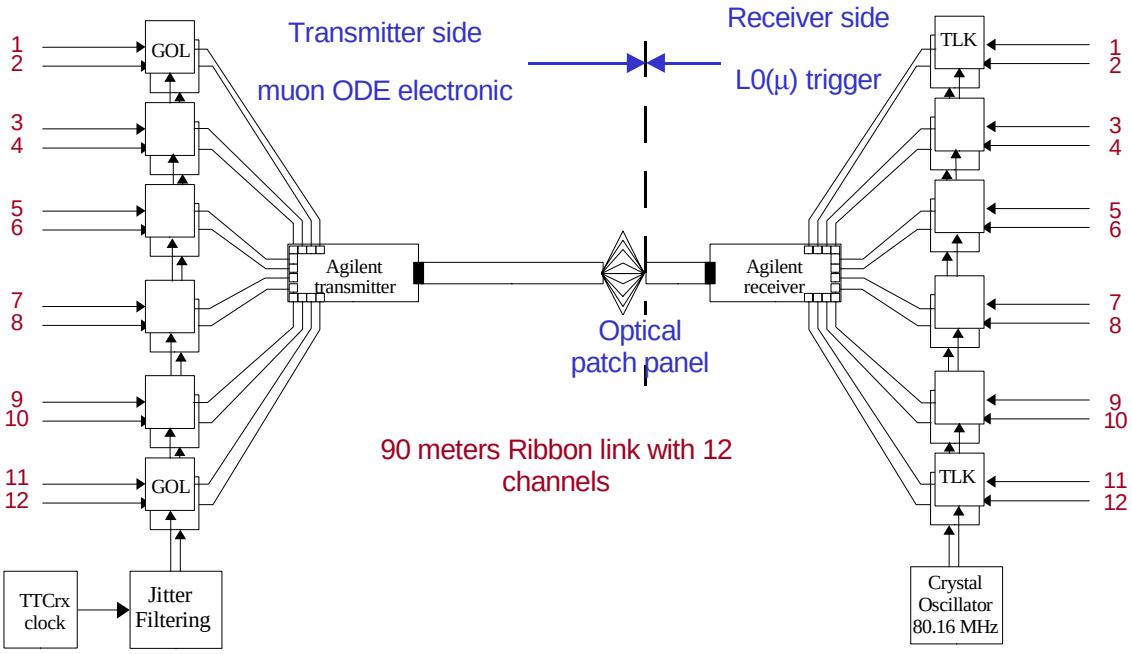


Figure 1 : Overview of Ribbon Optical Link

In the transmitter side :

- The serializer chip converts 32-bit data into 1.6 Gbit / s serial data ;
- The parallel optical transmitter from Agilent drives 12 optical links at 1.6 Gbit / s ;
- The jitter filtering circuit generates a low jitter clock compatible with the requirements of the high speed communications.

In the receiver side :

- The parallel optical receiver from Agilent receives 12 optical signals at 1.6 Gbit / s ;
- The deserializer recovers the original 32-bits data from the high speed signal.

After 90 meters, the optical ribbon cable is broken out in 12 individual fibers connected to a patch panel. In the other side of the patch panel, 12 individual optical links are merged into a ribbon cable connected to the level 0 muon trigger.

This optical distribution groups data coming from different stations and sends them to a single processing board.

We designed two boards to test and to characterize optical link running at 1.6 Gbit/s. There are based on the TLK2501 from Texas Instrument for serialization and deserialization. The first version is based on a single optical transceiver from StratosLightwave. The second one is based on the ribbon optical link from Agilent. In that set-up only one channel was equipped over the twelve. In the appendix, we provide a summary of those PCB boards. Devices having undergone radiation tests are clearly indicated.

2.1. Serializers and deserializers

In the L0 muon trigger, we have to integrate up to 24 deserializers in one 9U board. Thus, a low power consumption device is required.

The TLK2501 from Texas Instrument, based on sub-micron CMOS technology is the best candidate for this application. It converts a 16-bits parallel data word into a high speed serial data stream or vice versa.

The frequency range of the input clock is 80 MHz to 125 MHz corresponding to a serial data rate range between 1.6 Gbit/s and 2.5 Gbit/s. The power consumption of the TLK2501 is less than 300 mW.[2]

Another reason for this choice is the presence of a valid information transported with the data. This feature is very useful to synchronize data transmitted by several optical links.

The TLK2501 operates either in emission or in reception. On the emission side, it is possible to replace it by the GOL chip made by the CERN microelectronic group. This device uses the same transmission protocol as the TLK2501. It has been designed to be less sensitive to radiation effects [1].

The TLK2501 uses the 8B/10B code to convert each byte into a 10-bit word. This ensures a balanced count of transitions in the high speed serial data allowing the

2 In comparison, the G-link chip from Agilent consumes 2.5 W

receiver to recover the clock from the serial data.

The 8B/10B code provides two mirrored 10-bit words to represent one 8- bit data value. The difference between these words is the ratio of 1s to 0s. To select which of the two words to be sent, the transmitter evaluates the density of 1 and 0 bits in the previously sent word. If there is, for example, more 1s than 0s, the current data byte is encoded using the form with more 0s than 1s and vice-versa.

Consequently, the serial data are dc-balanced satisfying fiber optical interconnect requirements. In addition it can be easily interfaced with standard parallel optical fiber products.

The following steps are performed by the GOL or the TLK2501 on the emitter side:

1- Latch of the incoming data in reference to the input clock ;
2- Encode the data word with the 8B/10B protocol ;
3- Serialize the encoded data ;
4- Send the serial data onto a differential line using a Coupled Mode Logic (CML) driver.

On the receiver side, a TLK2501 performs the opposite operations in reverse order to regenerate to original sent word. In addition, a clock in phase with the received parallel data is extracted from the serial data stream.

The TLK2501 has a synchronization-state machine which is takes care of initialization and synchronization of the transmitter and receiver components. The initialization and synchronization state diagram is provided in the manufacturer data sheet [2].

The chip is able to auto-detect any loss of synchronization. In addition, the emitter and the receiver are able to resynchronize themselves in a few clock cycles. When the synchronization is lost, the state machine goes in a state indicating whether the invalid code received was caused by a spurious event or a loss of the link. In this case, the TLK2501 on the receiver side activates two flags to signal transmission errors to the level 0 muon trigger downstream logic.

Data sent by the TLK2501 are tagged by a “valid” flag. Before sending useful data, this valid flag is set to 0 on the emitter side. It is set to 1 when meaningful data are sent. The rising edge of the valid flag is used to synchronize several optical links together on the receiver side.

2.2. Optical transmitters and receivers

Several manufacturers (Agilent, Infineon, Zarlink ...) provide parallel optical devices running at up to 2.5 Gbit/s and driving 12 optical links in the same package. We chose Agilent devices because their jitter characteristic were better than its competitors.[3]

The HFBR-712BP transmitter and HFBR-722BP receiver from Agilent are high performance optical modules for parallel optical data communication applications. These 12-channel devices provide a cost effective solution for short distance communication (until 300 meters) and allow up to 30 Gbit/s aggregate bandwidth. These modules are designed to operate on multimode fiber at a nominal wavelength of 850 nm. The transmitter and receiver devices are housed in MTP/MPO packages. The power consumption is 1.5 W for the transmitter and 2.7 W for the receiver for all the 12 channels.

2.3. Optical ribbon fiber and connectors

Optical fibers operate in multimode at a wavelength of 850 nm.

To connect the muon detector front-end electronics to the muon processor, we use a ribbon of optical fibers with a MPO connector. The latter is the standard for parallel optical devices. Each ribbon contains 12 fibers.

At 90 meters from the muon detector front-end electronics, the ribbon cable is broken out in 12 single fibers as shown in Figure 1. The connectivity between individual fibers is obtained using SC-SC connectors mounted on a patch panel.

After the patch panel, 12 individual optical fibers are grouped into a ribbon cable which is connected to the L0 muon trigger.

3 At the time when the choice was made (end 2001)

3. Estimation of the theoretical Bit Error Rate

Good design practices in digital communication system consists in maximizing the bandwidth while minimizing the bit error rate.

The bit error rate depends on optical attenuation, jitter of serial data and on external system perturbations such as electromagnetic interference.

3.1. Optical power attenuation

The maximum power attenuation allowed for an optical link is called the loss budget. It is the sum of losses due to the length of optical fiber, connectors and splices.

The attenuation coefficient for the multimode 850 nm fiber, is 3.75 dB/km. Each connector pair introduces an attenuation of 0.75 dB and each splice an attenuation of 0.3 dB.

The typical distance between the muon detector front-end electronics and the muon trigger processor is 100 meters. We have 2 connection pair per link and 2 splices. This corresponds to a loss budget of 2.5 dB.

On the other hand, the minimum optical transmitter power is -8 dBm and the minimum receiver sensitivity is -16 dBm [3]. Thus, the power budget is equal 8 dB in the worst case. We have a margin of 5.5 dB making the attenuation effect on the bit error rate negligible. In the rest of this note, we will only consider the jitter effect.

3.2. Jitter issues

The choice of devices for an optical link is not arbitrary. We can select devices specified to work individually at a rate of 2.5 Gbit/s. But when components are chained together, the jitter cumulated along the chain might reach an unacceptable level. Thus, we have to select individual components keeping in mind the jitter budget for the whole chain.

The basic characteristic of digital communication is the synchronization between binary encoded data and their clock. The problem is how to preserve

synchronization from the transmitter to the receiver side when using serial data.

In an ideal system the error rate would be zero since the phase between the clock and the data is fixed and preserved along the whole chain. In real world, the edge of clock and the the positions of data bits fluctuates around their ideal position.

The time duration of one bit is called the unit interval (UI). The jitter budget is defined as the time allocated for one bit of data : 400 ps at 2.5 Gbit / s and 625 ps at 1.6 Gbit / s.

If the overall jitter of the chain, including jitter of all devices, is above the unit interval, the received data will be corrupted.

Jitter is divided into two fundamental types, called random and deterministic jitter.

Random jitter (RJ) is unpredictable and has a Gaussian probability density. It is caused by thermal or noise effects. Random jitter is normally described in term of the standard deviation value σ. The ratio α of the peak to peak value to standard deviation depends on the bit error rate required by the system as shown in Table 1. For example, if a bit error rate of 10^{-12} is required, the peak to peak value of the random jitter (RJ peak-to-peak) is 14 times the standard deviation.

Deterministic jitter (DJ) is caused by components interaction in the system especially the effect of limited bandwidth on specific patterns of 1 or 0 in the bit stream. Deterministic jitter is always described in term of peak to peak value.

Total jitter (TJ) is the combination of all random jitter and deterministic jitter components. In order to compute the total jitter, RMS jitter number for the random component is converted to peak to peak values. The total jitter is given by the linear sum of the peak to peak values of random and deterministic jitter.

BER	10^{-10}	10^{-11}	10^{-12}	10^{-13}	10^{-14}	10^{-15}	10^{-16}
α	12,72	13,41	14,07	14,7	15,3	15,88	16,44

Table 1 Gaussian waveform probabilities

3.3. Jitter budget of our configuration

3.3.1. Jitter of the serializer

To convert the parallel data word into a serial data stream, an internal phase locked loop (PLL) generates the internal high speed clock in phase with the user-supplied clock. The transmitter generates the serial data stream from this internal high-speed clock.

The output jitter has several sources:
- Jitter of the input clock ;
- Jitter generated by the PLL circuit ;
- Noise of the power supply.

In the TLK2501, the apparent bandwidth of the internal PLL is around 4-6 MHz. The PLL rejects the input clock jitter above this frequency and tracks the jitter below this frequency. Thus a part of input clock jitter is transferred to the high speed clock.

In the TLK2501, the transmitter peak to peak jitter is specified to be less than 80 ps or less if the power supply is clean and if the peak to peak jitter of the input clock is below 40 ps.

3.3.2. Jitter of the optical transmitter

For the optical transmitter, the total jitter is a combination of a random jitter and a deterministic jitter.

The jitter for HFBR-712BP Agilent optical transmitter is specified for a bit error rate of 10^{-12}. The typical peak to peak values are 20 ps for deterministic jitter and 60 ps for total jitter. The maximum peak to peak values are 60 ps and 120 ps respectively [3].

3.3.3. Jitter of optical fiber

Usually the jitter added by the fiber is mainly attributed to the inter-symbol interference. It is deterministic because it is determined by the transmitted data pattern. It depends essentially on the bandwidth of the fiber and it is generally

linear with the length.

The jitter added by a 100 meter fiber is estimated to 80 ps. This result was derived from measurements with different lengths of fibers.

3.3.4. Jitter of the optical receiver

In the HFBR-722BP data sheet, the jitter characteristics are specified through the stressed receiver eye opening value determined using a specific test pattern. The worst case value for this parameter is 130 ps at 2.5 Gbit/s [3].

The compatible Zarlink receiver has a similar stressed receiver eye opening value. Its deterministic and total jitter values are respectively 46 ps and 153 ps [4]. We assume that Agilent component has similar values.

3.3.5. Jitter of the deserializer

The deserializer recovers high speed clock from the incoming data stream. The high speed clock is used to strobe serial data. To avoid errors, the jitter of this clock must be as low as possible. As for the serializer, the noise of the power supply and input clock have to be very low.

The TLK2501 deserializer consumes itself a jitter budget corresponding to 40% of the bit time interval. It is specified to recover data correctly with up to 60% of eye enclosure.

3.3.6. Jitter budget calculation

When the overall jitter exceed the unit interval, the clock can not be extracted properly and the data transmitted contains a excessive number of errors. For this reason, it is necessary to check that the jitter budget of the chain doesn't exceed the critical value.

To obtain the total jitter we add linearly the deterministic jitter components and quadratically random jitter components.

For some components, only the total jitter is specified. In that case, the peak to peak value of the total jitter is calculated as the linear sum of the total jitter of

each component. This method over-estimates the total jitter.

System component	Total Jitter (p-p)		Deterministic Jitter(p-p		Random Jitter(p-p)	
	TJ (UI)	TJ (ps)	DJ (UI)	DJ (ps)	RJ (UI)	RJ (ps)
Serializer	0,13	80				
Optical transmitter	0,19	120	0,1	60	0,12	72
Fibre Added	0,13	80				
Optical Receiver	0,24	153	0,07	46	0,17	107
Summed jitter At deserializer input	0,57	433				

Table 2 : Optical Link jitter Budget calculation

Table 2 shows that the total jitter is 0.57 UI at the input of the deserializer. This corresponds to an opening eye diagram of 0.43 UI which is higher than the 0.4 UI required by the deserializer for clock recovery. Thus, we conclude from this evaluation that the optical link has a bit error rate lower than 10^{-12} at 1.6 Gbit/s in the worst case *when the jitter of the input clock is lower than 40 ps.*

3.3.7. Clock jitter

One of the most important issues for the design of the high speed data transfer is the quality of the input clock. On the emitter side, this clock provides the reference clock for the internal PLL which is multiplied by a factor 20 to generate the high speed clock. The rising edge of the internal high speed clock is continuously compared to the input clock. The PLL will speed up or slow down the voltage controlled oscillator frequency in the TLK2501 in order to keep these two signals phase aligned.

Thus, the input clock must be jitter free as much as possible in order to minimize jitter introduced into the high speed clock and latter in the high speed data stream.

For the TLK2501 the jitter of the input clock has to be lower than 40 ps peak to peak to guarantee an acceptable bit error rate [2] [11].

The 40.079 MHz bunch clock output provided by the TTCrx has a jitter of about 300 ps peak to peak [12]. Such jitter does not match requirements of a high speed optical link. Thus, the TTCrx clock can not drive directly any serializer or deserializer running at 1.6 Gbit/s. The bit error rate measurements for the link driven by TTCrx clock confirm this : we obtained a value of 10^{-3}. In the next section, we present a scheme to reduce the jitter of the TTCrx clock to an acceptable level for the high speed optical link.

4. A solution to filter the TTCrx jitter

In this section, we describe a scheme to filter the TTC clock in the emitter side and in the receiver side.

4.1. Emission side

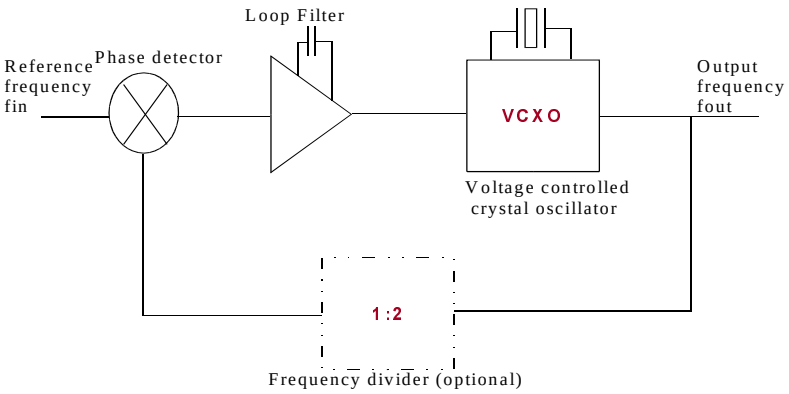


Figure 2 : Narrow bandwidth PLL based on the VCXO for jitter filtering

The most common technique to filter jitter is shown in Figure 2. It uses a narrow bandwidth phase locked loop which is locked to the incoming reference clock.

The PLL acts as a low pass filter for the high frequency fluctuations of the reference clock. Because of the low pass filter, the PLL is able to follow the slow drifts of the reference clock.

However, the voltage controlled crystal oscillator (VCXO) has an internal jitter that cannot be eliminated with the current set-up.

To reach a value of jitter as low as 40 ps peak to peak, we must use a VCXO with a very low phase noise.

When we use the TLK2501 instead of the GOL chip, we have to double the clock frequency because the data path is 16 bits for the TLK2501 and 32 bits for the GOL. This is why we insert an optional divider by 2 in the loop of the PLL.

4.2. Reception side

In the reception side, the TLK2501 requires an input clock with a low jitter (<40 ps peak-to-peak). This clock do not have to be in phase with the TTCrx clock. Then, we can use a simple low noise crystal oscillator to drive the TLK2501. The only constraint is relative to the stability of the crystal oscillator with respect to the aging and temperature fluctuation. The frequency has to be stable within 200 ppm compared with the TTCrx clock frequency.

4.3. Clock distribution to several devices

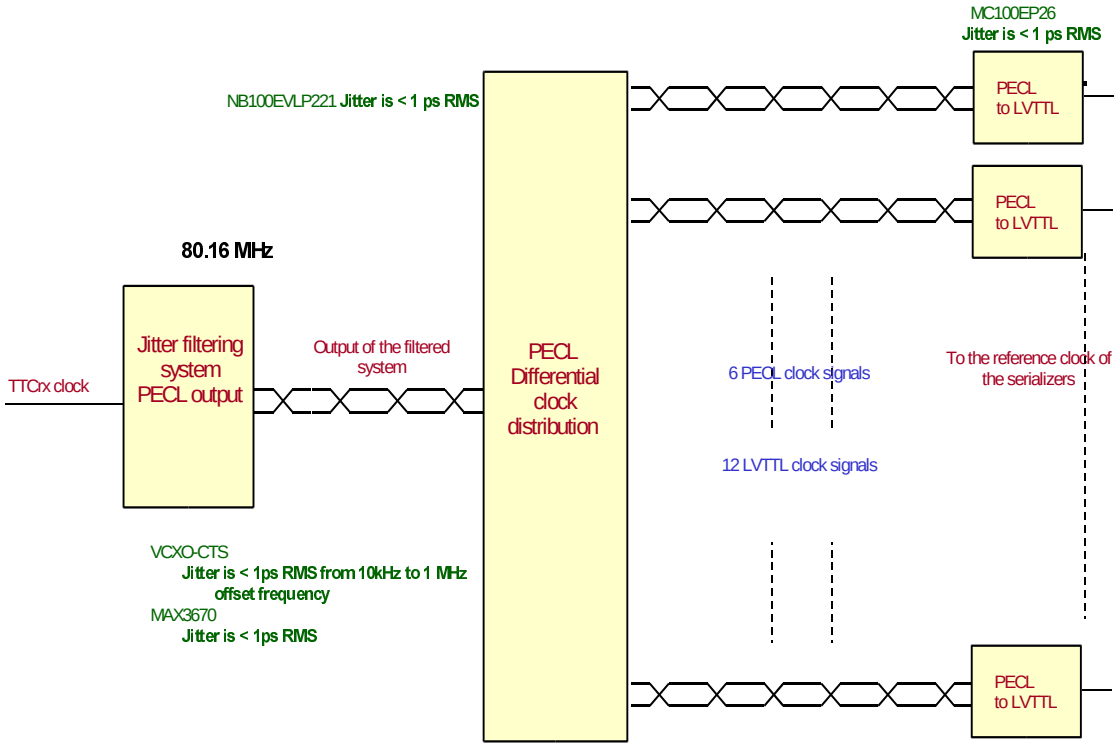


Figure 3 : Clock distribution technique

In our system, we have to distribute a clock with a very low jitter. The clock distribution system is designed as shown in Figure 3 to preserve this low jitter.

We use PECL logic which provides some benefits over CMOS logic in high speed

applications :

- PECL produces fast rise and fall times and the output signal has a fast transition time around the transition region well suited to minimize the jitter;
- PECL technology eliminates common mode noise by offering differential inputs and outputs.

PECL to CMOS translation is required since the TLK2501 has a CMOS input clock. It is important to locate each translator close to the load in order to maintain good signal integrity. We are using the NB100EVL110 clock distributor circuit and the MP100EP26 PECL/CMOS translator. These components from OnSemiconductor add in the worst case a jitter of 1 ps RMS.

The RMS value of the resulting jitter at the input of the serializer is calculated as the quadratic summation of RMS values of jitter introduced by all devices in the clock path including the clock distributor and translator circuits.

If we assume that the clock at the output of the TTC filtering system has a jitter of 4 ps RMS, the jitter of the clock at the input of the serializer will be below 4.3 ps RMS.

5. Board layout considerations

When implementing a 1.6 Gbit/s serial link, the layout of the printed circuit board (PCB) has to follow specific design rules for high speed signal and clock lines and for power supply and bypass capacitors.

The high speed signal rise and fall times are less than 200 ps. The input clock rise and fall times are less than 1 ns. Careful attention to trace lengths and routing will prevent signal ringing. A solid plane ground and power plane are useful in distributing a clean power and preventing additional jitter on high speed signals and clock.

In our design, we follow these general rules :

1. keep traces as short as possible ;
2. Use controlled impedance for traces terminated by matching resistor to prevent reflections ;
3. When routing differential pairs, keep the trace identical between the two traces to prevent signal skew ;
4. Use rounded corners rather than 90 or 45 degrees corners ;
5. Use the power/ground planes as an effective power supply decoupling. The capacitance of the planes is more effective than a capacitor component because it has no inductance or series resistance ;
6. Use an LC filter with a ferrite bead inductance to bypass analog power supplies. The used transceivers have internal PLL powered separately which are particularly sensitive to the noise. Power supply filtering method has a significant impact on the signal quality and on the jitter performance.

6. Experimental Results

The test bench designed to characterize the optical link allows to estimate the bit error rate of the optical link.

In this section, we present the performances of the optical link as a function of optical attenuation, power supply noise and input clock jitter.

We will also present the performances of the clock jitter filtering system designed to make the TTC clock compatible with high speed link requirements. Finally, we give the sensitivity to single event upsets for all devices involved in the emission side excepted the ribbon transmitter.

6.1. Bit error rate estimation methods

We use two methods to estimate the bit error rate of the optical link:

- The pattern generator method shown in Figure 4, where the emitter sends a known data sequence to the receiver side. Errors are computed in real time at 80 MHz ;
- The eye diagram display method.

6.1.1. Pattern generator method

In the transmitter side, the FPGA is programmed as a 2^{31}-1 pseudo-random data generator. It is driven at 80 MHz and generates 16 bits parallel data. These 16-bits data are serialized into one data stream by the serializer and transmitted on optical fiber using the Agilent optical transmitter.

In the receiver side, the optical high speed signal is converted to an electrical one using the Agilent optical receiver. The high speed signal is then demultiplexed to 16-bit parallel data. These data are then compared to the same pseudo-random generator as the one implemented on the transmitter side.

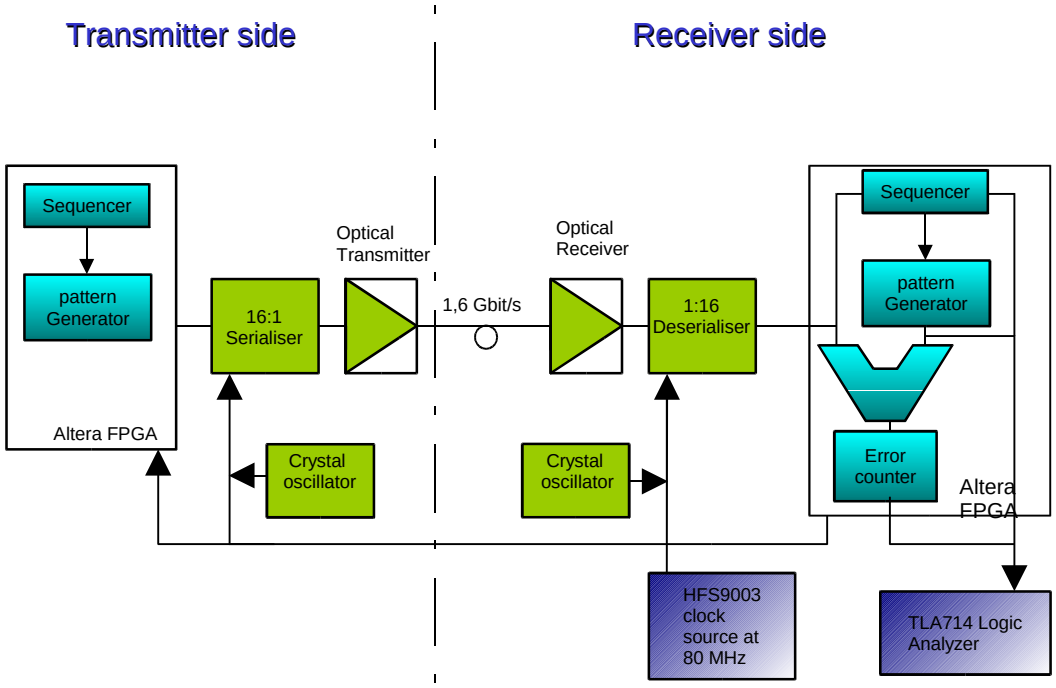


Figure 4 : Optical link test board and bit error rate estimation method

The bit error rate is computed as the ratio of corrupted bits to good bits. The serializer and the deserializer use the 8B/10B coded protocol. When an error is detected, the bit error rate tester does not differentiate between a single bit error and multiple bit errors for a single word. The number of corrupted bits can be comprised between 1 and 16 bits. We consider to be always in the worst case as if all the 16 bits have flipped.

The bit error rate is thus given by : $BER = \frac{N_C}{N_T}$, where N_C is the number of words corrupted and N_T is the total number of words transmitted at 1.6 Gbit/s.

If the mean time between errors is one hour, the bit error rate is 3.47×10^{-12}. Thus, if we want to measure a bit error rate with a high level of confidence, we have to run this test during a long period.

Measuring a bit error rate at a level of 10^{-14} requires to run the link during several weeks.

To reduce this time or to access to a lower bit error rate, we use another method based on the eye diagram display.

6.1.2. Eye Diagram and jitter measurement method

The performance of the optical link is often evaluated using the eye diagram display. The quality of the eye diagram depends on the input signal and on the trigger source.

The most precise technique is to trigger the oscilloscope with a clock at the same speed as the serial bit rate. Unfortunately, this clock is not accessible in the TLK2501 deserializer. For this reason, a specific clock recovery is included in some oscilloscope. We take the 80 MHz clock used for serialization since we do not have such equipment.

This 80 MHz clock used as trigger can provide inaccurate results if it exhibits itself some jitter. We have to take care to use a very low jitter clock.

In addition, some care must be taken on the data pattern used. The data rate to clock speed ratio is 20 ; if the rising edge of the 80 MHz clock is in phase with the bit 1, the next rising edge will be in phase the bit 21 and etc. Thus, triggering on the rising edge of the 80 MHz clock produces an incomplete eye diagram if the words are composed of a fixed pattern. To obtain a complete eye diagram we must use random patterns.

Measuring the opening of the eye diagram at the input of the deserializer, gives access to a quantitative estimation of the bit error rate, because of the correspondence between RMS value of jitter and error rate as shown in Table 1.

6.2. Measurements of the bit error rate

6.2.1. Test bench setup

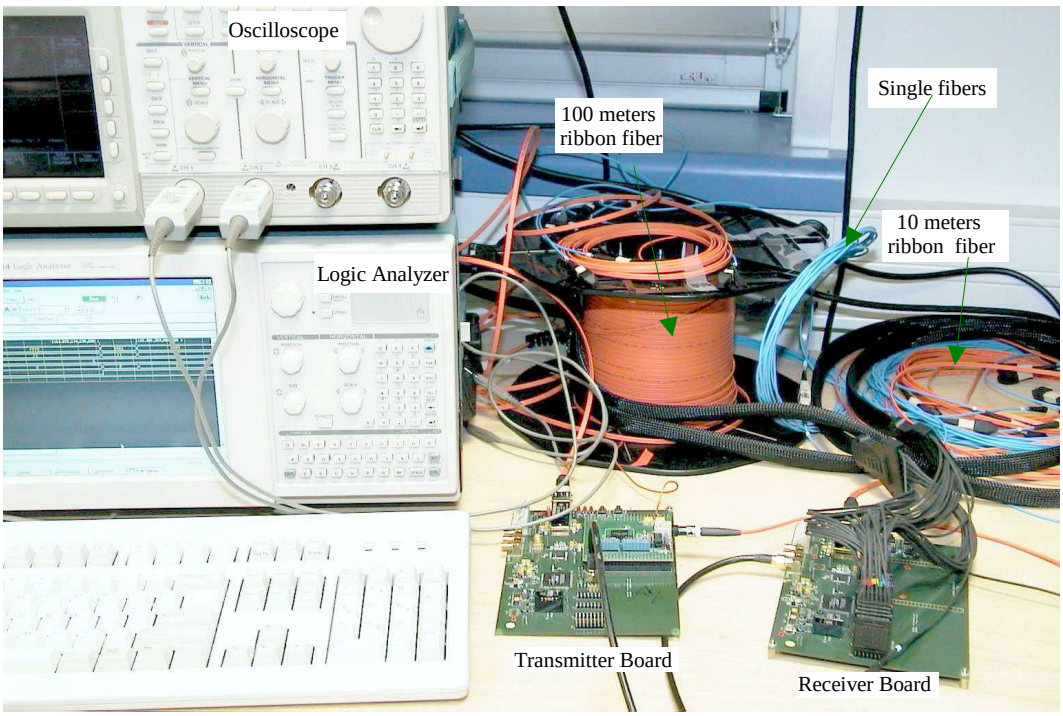


Figure 5 : Optical link test bench

Figure 5 shows the test bench built to characterize the high speed optical link.

A logic analyzer (TLA714) is running in transitional mode to capture the errors. It is possible to store all errors with a corresponding time stamp.

A clock generator (HFS9003) is used as a clock source for the serializer and for the deserializer. This allows to test the link at bit rates from 1.6 Gbit/s to 2.5 Gbit/s.

A sampling oscilloscope (TDS694C) has a 3 GHz analog bandwidth and a 10 GS/s sampling rate. The effective bandwidth is 2.40 GHz since we use a 4 GHz bandwidth active probe. This means that the oscilloscope and probes can correctly display signals with rise-times not faster than 145 ps

(t_{rise} = 0.35 / bandwidth). We can note that the output signal of the TLK2501 transmitter have typically 150 ps rise and fall times.

6.2.2. Bit error rate in standard conditions

The link prototype was tested using the pattern generator method, from bit rate of 1.6 Gbit/s to 2.5 Gbit/s. At 1.6 Gbit/s, the test was done continuously during 10 days without errors. Over 1.3×10^{15} bits were sent, received and checked by the bit error rate tester integrated in the FPGA. This error free time yields an estimate of bit error rate around 10^{-14} .

6.2.3. Sensitivity of our setup to optical attenuation

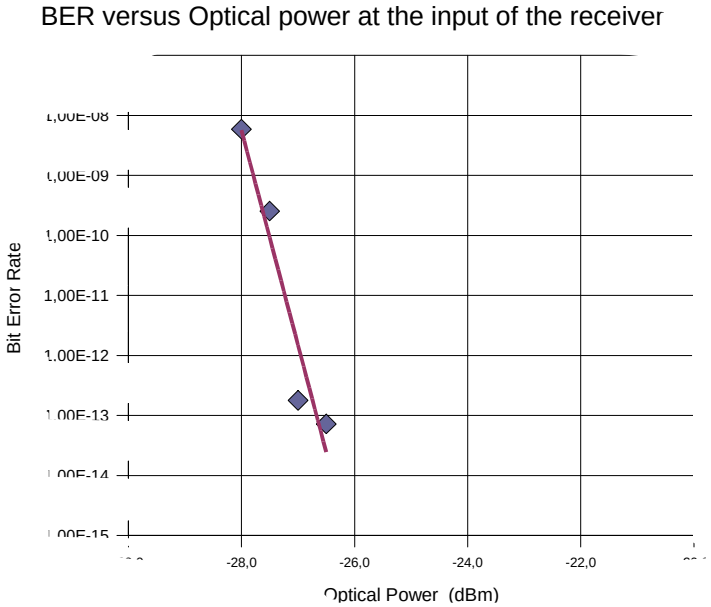


Figure 6 : Bit error rate versus optical power at the input of the optical receiver

Figure 6 shows the bit error rate as a function of the optical power at the input of the optical receiver.

In normal operation, the measured optical power is -12.4 dBm for a fiber length of 100 meters. Thus, the bit error rate of our configuration can be can be extrapolated well below 10^{-15}.

6.2.4. Sensitivity of our setup to power supply noise

Power supply noise and ripple could be sources of errors in optical links. Externally generated noise can pass through power supply and reach serializer / deserializer as well as optical devices.

We tested the influence of the power supply on the bit error rate by superimposing a 2 Volt peak to peak high frequency signal to the power supply. In this case the measured power supply noise is 408 mV peak to peak as shown in figure 7. Bypassing techniques implemented in the board maintain this noise under 140 mV.

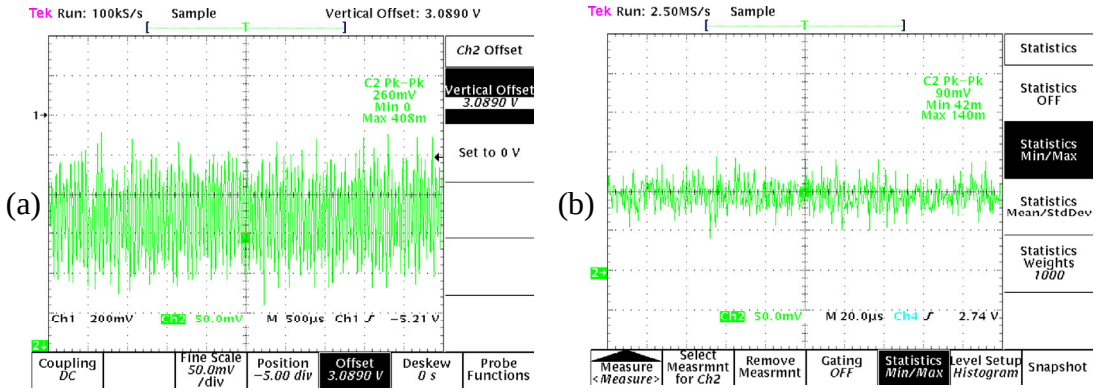


Figure 7 : Effect of bypassing techniques on the the power supply noise
(a) : Injected power supply noise
(b) : Noise measured at the power supply pin device

We obtain an excellent noise immunity against power supply as shown by the measured eye diagrams in Figure 8 .

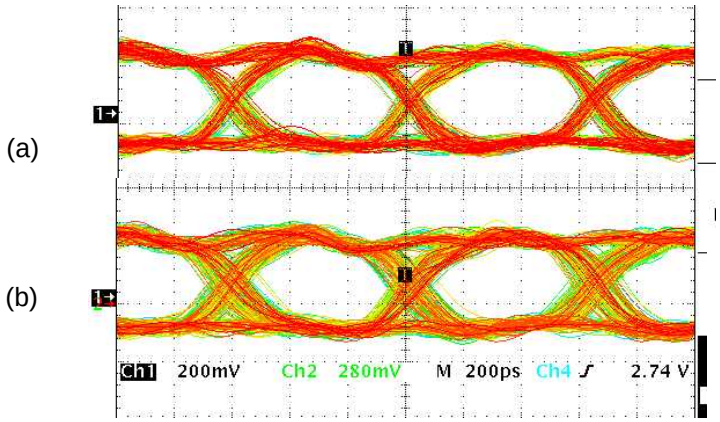


Figure 8 : Influence of the power supply noise on the quality of the link
a) Eye diagram without noise added to the power supply
b) Eye diagram with 408 mV noise superimposed to the power supply

6.2.5. Sensitivity of our setup to clock jitter of the emitter side

	Quartz oscillator from Pletronix	Quartz oscillator from Saronix	HFS9003 clock generator	Lecroy generator	TTCrx clock
Clock jitter **(peak-to-peak)**	50 ps	130 ps	120 ps	250 ps	300 ps
Deserializer input jitter **(peak-to-peak)**	194 ps	256 ps	228 ps	440 ps > 0.5 UI (312 ps)	>0.5 UI (312 ps)
Bit Error Rate at 1.6 Gbit/s	Very low	Very low	$< 10^{-14}$	$\sim 10^{-3}$	$\sim 10^{-3}$

Table 3: Bit error rate versus clock jitter

Table 3 shows the measurements of bit error rate as function of the input clock jitter. When it is driven by the TTCrx, the bit error rate becomes unacceptable. A clock jitter filter is then mandatory.

6.3. Performances of the jitter filtering circuit

Jitter is defined as the deviation of the edge location from their ideal positions. Clock jitter measurements can be classified in three categories : cycle to cycle jitter, period jitter and phase jitter [10].

- Cycle to cycle jitter $t_{jit(cc)}$ is the difference in the period of any two adjacent clock cycles. Cycle to cycle is usually measured over some large samples of cycles and specified as the maximum difference. This jitter is also referred as short term jitter.

- Period jitter $t_{jit(per)}$ is defined as the deviation in cycle time with respect to an ideal period. When measured over a long time period, this jitter type is reported as an absolute maximum value.

- Phase jitter $t_{jit(\Phi)}$ is defined for PLL based clock drivers. This values the difference between the reference input and the phase of the feedback output.

Value of jitter may be given as RMS or peak to peak number. They may be

typical or maximum values.

Jitter is measured over a large number of samples. The data for a typical device when plotted represents a classical Gaussian distribution.

Confidence factor	0.683	0.9545	0.9973	0.999937	$1-1.97\acute{}10^{-7}$	$1-1.24\acute{}10^{-13}$
(peak-to-peak)/σ	+/-1	+/-2	+/-3	+/-4	+/-5	+/-6

Table 4 : Confidence factor versus the peak to peak value for the Gaussian distribution

RMS value listed in some component data sheet represents a one sigma deviation above and one sigma deviation below the mean value. The peak to peak value is derived from RMS value with a corresponding confidence factor. Table 4 lists the confidence factor corresponding to the peak to peak value.

Plus or minus 5 sigma seems to be a good assumption for the peak to peak value.

6.3.1. Jitter measurements Test set-up

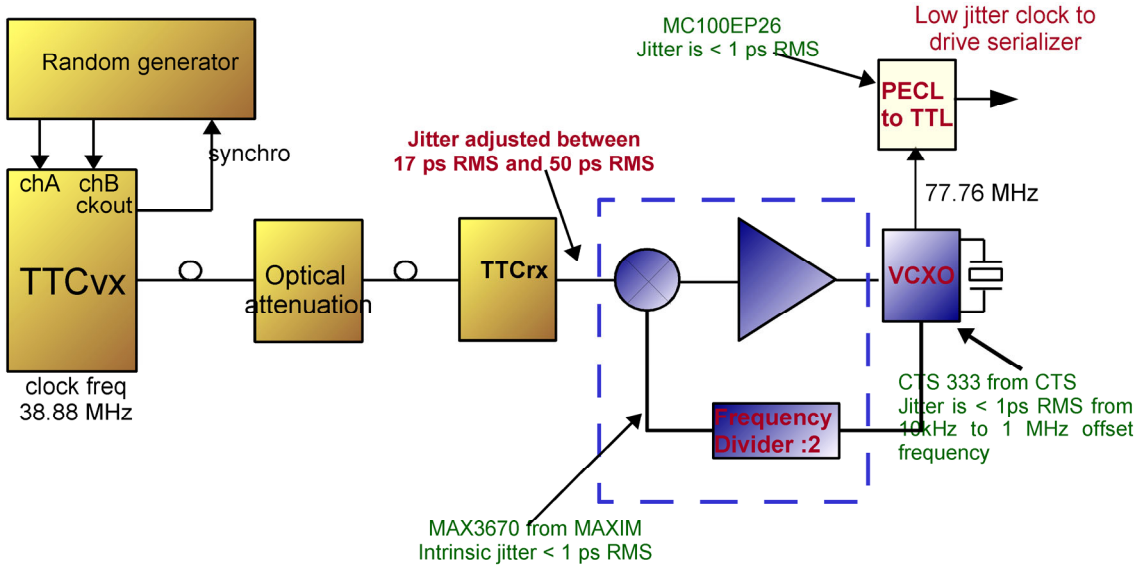


Figure 9 : Test set-up for jitter measurements

Figure 9 shows the test set-up realized to test the jitter filtering circuit. The TTCrx mezzanine board was installed on our prototype board. The 40 MHz TTCrx clock

drive the frequency multiplier based on the Maxim PLL (MAX3670) [6] and low phase noise VCXO (CTS333) [7]. The 80 MHz low jitter clock drives the TLK2501 serializer.

This filtering system is only based on commercial devices. It would be replaced by the QPLL ASIC designed by the CERN Microelectronic group using radiation tolerant layout practices to meet the LHC radiation requirements [8].

The TTCrx module is connected to the TTCvx board through a 5 meter optical fiber.

The TTCrx clock jitter depends on the level of signal received on its optical input signal and depends also on the rate of activity in channel A and channel B. These channels are used to broadcast control words and the trigger information in the TTCvx.

In order to vary the rate of jitter, we use:

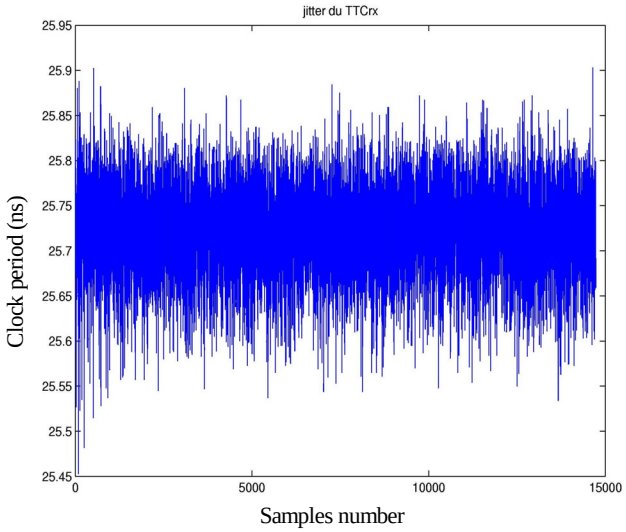
- An optical attenuator (HP8158B) between TTCvx and the TTCrx boards to adjust the signal level at the input of the TTCrx module ;
- A random generator (HFS9003) synchronized to the TTCvx to adjust the activity rate in channel A and channel B for the TTC vx module.

Since we would like to reach a value of jitter as low as 4 ps RMS corresponding to 40 ps peak-to-peak, the jitter analysis equipment has to be very precise. We use the TDS694C oscilloscope including specific a software (TDSJIT1V2). It is based on single-shot jitter measurements [13]. Such a technique makes the measurement process independent of the oscilloscope trigger jitter. The timing accuracy for the TDS694C is 3 ps RMS for a sampling rate of 10 GS/s and it is able to measure down to 1.5 ps RMS jitter.

6.3.2. TTCrx jitter measurements

For an optical input level at the TTCrx of -38 dBm and a high activity rate in channel A and channel, the measured jitter is 48.2 ps RMS and 450 ps peak-to-peak as shown in Figure 10 representing the jitter histogram at the output of the TTCrx shows module.

When there is no broadcast control words and for 5 meters of fiber between TTCvx and TTCrx module without any optical attenuation, this jitter is only 17 ps RMS (~170 ps peak-to-peak).



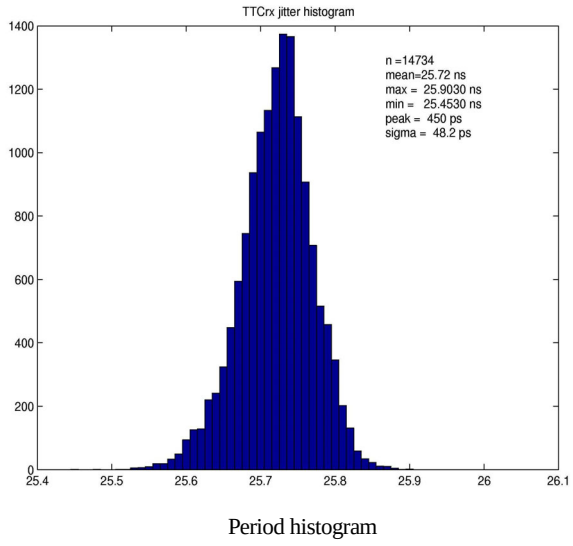


Figure 10 : TTCrx Jitter measurements

6.3.3. Jitter filtering clock measurements

The jitter filtering system was tested using the test set-up illustrated in Figure 9. The PLL bandwidth is maintained as narrow as possible.

Figure 11 shows the output jitter versus the input one. The jtter of the filtered clock **remains around 10 ps RMS** when the TTCrx jitter varies from 17 ps RMS to 48 ps RMS.

Reducing again this value would require to use a very low noise VCXO as the S1559 from Saronix[4] [9]. The jitter of the filtered clock will then be as low as the jitter required by the TLK2501 serializer.

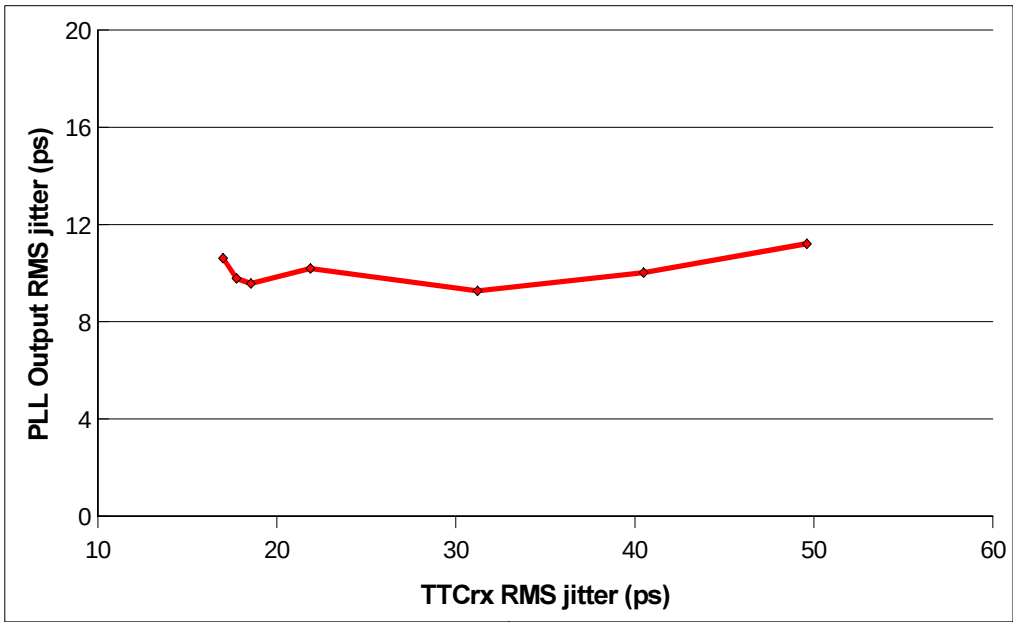


Figure 11 : PLL output jitter versus the TTCrx jitter

6.3.4. Optical link driven by the filtered clock

The input clock of the deserializer is now driven by the filtered clock. The link was tested for several hours without errors.

4 As it was not possible to get this device in small quantities, we have not tested it in the current set-up

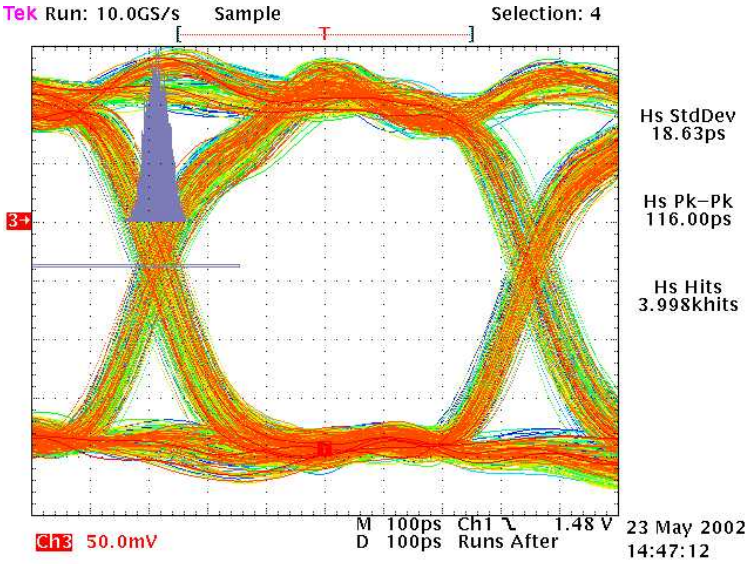


Figure 12 : Eye diagram at the deserializer input

(The serializer is driven by the filtered clock)

Figure 12 shows the eye diagram measured at 1.6 Gbit/s. The RMS value of the jitter is about 18.6 ps.

At 1.6 Gbit/s, 0.6 UI corresponds to 375 ps which is higher than 17 times the measured RMS jitter value. This corresponds to a bit error rate lower than 10^{-16} as shown in Table 1.

We confirm that the low phase noise clock is a key parameter to ensure a low bit error rate in the high speed optical links.

6.4. Radiation effects measurements

Radiation effects in the transmitter devices can affect the performance of the high speed optical link. This can result in an increase of the bit error rate of the optical link.

The three basic effects that should be considered are effects due to the total ionizing dose (TID), displacement damage and single event effects.

6.4.1. Radiation environment in the muon front-end

In the muon environment, the deposited TID is less than 8 krad as shown in Table 5. The threshold level for TID-induced failure is generally above this level for the modern commercial devices.

	1 MeV Neutron Eq. (10 years) (part/cm²)	Hadrons > 20 MeV (10 years) (part/cm²)	Total Dose (rad) (10 years)
M1-ODE	9.8×10^{11}	5.0×10^{10}	7.9×10^{3}
M2-ODE	3.4×10^{11}	1.9×10^{10}	2.2×10^{3}
M3-ODE	1.8×10^{11}	7.9×10^{9}	680
M4-ODE	1.9×10^{11}	5.3×10^{9}	390
M5-ODE	2.6×10^{11}	4.5×10^{9}	320

Table 5: Radiation levels in the muon environment[14]

The displacement damage is a long term degradation of device performance and leads to device failure. bipolar components and particularly optical components are subject to displacement damage. Therefore, they have to be tested under a total fluence comparable with the expected equivalent 1 MeV neutron fluence given in Table 5.

Single event effects tests using protons were performed at two facilities : the Cyclotron Research Center (CRC) Louvain la Neuve and the Paul Scherrer Institut (PSI) at Villigen. Proton test energies incident on the tested devices are listed in Table 6. Typically, the the devices were irradiated to a fluence from 1×10^{12} to 3×10^{12} particles / cm².

During two campaigns in June 2001 and in November 2002, we irradiated the TLK2501, the GOL chip, a single optical transmitter (MLC25-8-1-TL from Stratos [5]) and all the components entering in the jitter filtering circuit. Unfortunately, we did not test a ribbon optical transmitter since one of our power supplies failed at the beginning of the irradiation.

Facility	Particle	Particle Energy (MeV)	Flux (particles /cm²/s)	Irradiated devices	Total fluence (particles /cm²)	Total dose (krad)
Cyclotron Research Center (CRC) UCL - Louvain La neuve)	Proton	63 MeV	3.5×10^{8}	TLK2501	1.0×10^{12}	140
				GOL device	3.14×10^{12}	440
				Single Optical transmitter	1.7×10^{12}	238
Paul Scherrer Institut (PSI) Villigen	Proton	250 MeV	5.0×10^{8}	MAX7036	1.6×10^{12}	96
				CTS333	1×10^{12}	60

Table 6 : Radiation test

6.4.2. ODE transmitter devices irradiation

The bit error rate test bench described previously in Figure 4 was used to detect errors introduced by upsets. They were displayed and recorded in the logic analyzer with time stamp information and data error duration.

During the tests, a high fluence was reached to improve the statistics of SEU occurrence.

During the tests, the power consumption was monitored for single event latch-up (SEL) or other destructive effects. It represents also an indication about the influence of the total ionizing dose effects on the device.

From the tests results, we have distinguished two categories of upsets :

- Short burst of bit errors with time duration of a few clock cycles at 80 MHz ;
- Long burst of bit errors with time duration of several thousands of clock cycles at 80 MHz.

There are two explanations for the long burst of bit errors :

- The single event upset causes a corruption of high speed data stream and the clock recovery circuit could not lock on received data. Erroneous data are transmitted as long as the clock recovery circuit in the serializer or the deserializer is disturbed. This kind of errors is detected by the 8B/10B encoding circuitry because invalid codes are transmitted.

- The single event upset causes a corruption in the clock signal supplied by the

jitter filtering circuit. The frequency lock is lost for a time duration corresponding to the response time of the Maxim PLL device. In this case, errors are not detected by the 8B/10B encoding circuitry. Indeed, the optical link is not down but it runs at the free frequency of the voltage controlled oscillator. Errors are introduced by the data misalignment. When the PLL is locked again, the misalignment persists up to the end of the current machine cycle : in the level 0 muon trigger, data are time aligned at the beginning of each machine cycle.

The goal of this irradiation tests is to measure the individual single event upsets cross section for each device involved in the optical part in the transmitter side. It allows to estimate the SEU rate in a given radiation environment.

One SEU can introduce a long burst of errors during a time much higher than a bit duration. Thus, the optical link is characterized by the *bit error cross section* defined as the total number of erroneous bits divided by the total proton fluence [15].

6.4.2.1. The TLK2501 serializer irradiation

Two TLK devices were irradiated at Louvain to measure the cross section. For this test, the proton flux was adjusted at 3.5×10^{8} particles/cm^2/s .

For a total proton fluence of 2×10^{12} /cm^2, which corresponds to 2857 seconds per device, 8 events were observed during the first device test and 11 events during the second one. Therefore, the cross section of the TLK2501 could be estimated to 0.95×10^{-11} cm^2/device.

Among these 19 observed upsets for the two devices:

- 11 upsets introduced an error in the data directly. The average of the dead time was three 80 MHz clock cycles per upset. This results in 528 bits corrupted during this test.
- 8 upsets introduced a clock recovery failure. The dead time in this case was 30,000 clock cycles per upset. This results in 3890000 bits corrupted during this test.

The corresponding bit error cross section is estimated to 2.6×10^{-6} cm^2.

During the tests, the power supply current was monitored. An in situ supply current measurement was made. A significant change was observed in the TLK2501 device supplied current as shown in Figure 13. This is due to the total

ionizing dose. The TID effect will be negligible in the muon environment since we expect a maximum of 8 krad over ten years.

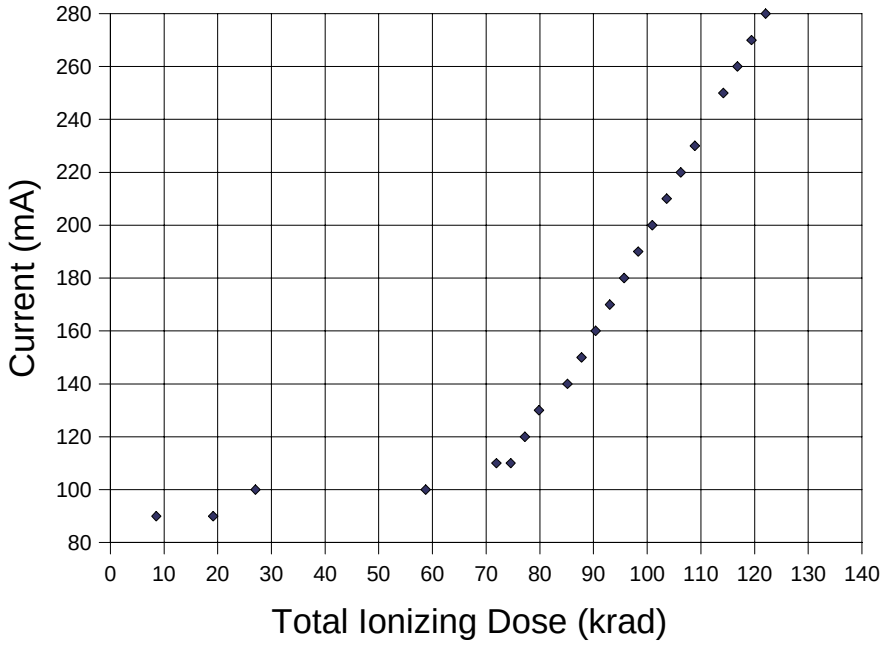


Figure 13: TLK2501 supply current variation in function of the TID

6.4.2.2. GOL chip irradiation

This chip was tested by Paulo Moreira from CERN's Microelectronics group under the same conditions as the TLK2501. For a total fluence of 3.14×10^{12} particles/cm^2, no bit data upsets or clock upsets were observed. The cross section can be estimated lower than 3.2×10^{-13} cm^2/device. No changes were observed on the supplied current during the experiment [16].

6.4.2.3. Single optical transmitter irradiation

The proton irradiation of the MLC25-8-1-TL chip from StratosLightwave was done in the same conditions as the TLK2501. Since, the total dose had no significant effect on the supplied current, we reached a total fluence of 1.7×10^{12}/cm^2 for this device.

34 upsets were observed during proton irradiation. The cross section is then 2.0×10^{-11} cm^2/device. Two categories of upsets occurred:

- 25 upsets introduced an error in the data directly. The average of the dead time was three 80 MHz clock cycles per upset

- 9 upsets introduced a clock recovery failure. The dead time in this case was 30,000 clock cycles per upset.

The measured bit error cross section is equal to 3.0×10^{-7} cm^2.

6.4.2.4. The Maxim PLL irradiation

Proton tests for the MAX3670 were performed at PSI in November 2002. The device was irradiated with proton fluence of 1.6×10^{12} particles/cm^2. We observed 139 upsets during this test. Thus, the total upset cross section is 8.7×10^{-11} cm² per device. The bit error cross section is equal to 8.34×10^{-5} cm^2.

The most severe error we observed corresponds to a loss of lock of the PLL during up to 3 ms.

6.4.2.5. The voltage controlled crystal oscillator irradiation

Proton tests were performed in the same conditions as for the MAX3670 device. The device was irradiated with a proton fluence up to 1.0×10^{12} particles/cm². We observed 8 upsets during this test. Thus, the total upset cross section is 8×10^{-12} cm². The bit error cross section is equal to 9.0×10^{-10} cm^2.

6.4.3. Optical link response to the radiation in the muon environment

The results of single event upsets tests are summarized in the Table 7. The total bit error cross section of the ODE transmitter is estimated from cross sections of each component. In this evaluation, we assume than an ODE board is equipped with 12 single optical transceivers.

From the total bit error cross section, we determine the total number of errors in the muon environment. Knowing the total number of transmitted bits, we are able to calculate the equivalent bit error rate of the high speed optical link.

	Fluence (protons/cm²)	Dose (krad)	SEU (Number of events)	Mean dead time /SEU (LHC cycle)	Cross-section (cm²)	Bit-error cross-section (cm²)
TLK serializer	1.0×10^{12}	140	11 (8)	2.1	0.95×10^{-11}	2.6×10^{-6}
GOL serializer	3.14×10^{12}	440	0	2.1	3.2×10^{-13}	7.6×10^{-8}
Single Optical transmitter (StratosLightwave)	1.7×10^{12}	238	34	1.0	2.0×10^{-11}	3.0×10^{-7}
MAX3670 (Maxim PLL)	1.6×10^{12}	96	139	8.4	8.7×10^{-11}	8.34×10^{-5}
VCXO (CTS)	1.0×10^{12}	60	8	0.01	8.0×10^{-12}	8.96×10^{-10}

Table 7 : Measured cross sections for the transmitter devices

The ODE transmitter contains 12 channels. For an ODE transmitter based on the GOL chip and the single optical transmitter, the single event upsets cross section of the emission chain is given by:

$$\sigma_{SEUtot} = 12\ \sigma_{SEU\_GOL} + 12\ \sigma_{SEU\_OptTr} + \sigma_{SEU\_MaxPll} + \sigma_{SEU\_VCXO} = 3.4\times10^{-10}\ cm^2$$

since we have 12 GOLs, 12 optical transmitters and 1 jitter filtering circuit.

As shown in table 8, in the muon environment the total number of SEU is estimated to be less than 2 SEU per year per ODE transmitter.

For the whole muon detector which contains 168 ODE boards, the total number of SEU is estimated to 2.5 SEU per day.

	Hadrons>20 MeV (10 years) (part/cm²)	Total Cross-section (cm²)	SEU (events per year)	Mean dead time per SEU (LHC cycles)
M1-ODE	**5.0×10^{10}**	**3.4×10^{-10}**	**1.70 ± 0.2**	**3**
M2-ODE	1.9×10^{10}	3.4×10^{-10}	0.65 ± 0.1	3
M3-ODE	7.9×10^{9}	3.4×10^{-10}	0.27 ± 0.03	3
M4-ODE	5.3×10^{9}	3.4×10^{-10}	0.18 ± 0.02	3
M5-ODE	4.5×10^{9}	3.4×10^{-10}	0.15 ± 0.02	3

Table 8 : Number of SEU in the muon environment

As the jitter filtering circuit drives 12 channels, the total bit error cross section of the emission chain is given by:

$$\sigma_{BERtot} = 12\ \sigma_{BER\_GOL} + 12\ \sigma_{BER\_OptTr} + 12\ \sigma_{BER\_MaxPll} + 12\ \sigma_{BER\_VCXO} = 1.0\times10^{-3}$$

Using the calculated bit-error cross section, the total number of errors is equal in the worst case to 5×10^{7} bits for ten years. The total number of transmitted bits in ten years for 12 links is 1.5×10^{18} bits. Thus, the equivalent bit error rate is estimated in the worst case to be less than 3.3×10^{-11} as shown in Table 9.

	Hadrons>20 MeV (10 years) (part/cm²)	Total bit -error cross-section (cm²)	Total number of errors	Equivalent Bit Error rate BER
M1-ODE	**5.0×10^{10}**	**1.0×10^{-3}**	**5.0×10^{7}**	**3.3×10^{-11}**
M2-ODE	1.9×10^{10}	1.0×10^{-3}	1.9×10^{7}	1.2×10^{-11}
M3-ODE	$7.\times10^{9}$	1.0×10^{-3}	7.9×10^{6}	5.2×10^{-12}
M4-ODE	5.3×10^{9}	1.0×10^{-3}	5.3×10^{6}	3.5×10^{-12}
M5-ODE	4.5×10^{9}	1.0×10^{-3}	4.5×10^{6}	2.9×10^{-12}

Table 9 : The equivalent bit error rate in the muon environment

The laser driver of the optical ribbon transmitter has 12 independent channels. However, if we assume that 12 channels of the ribbon optical transmitter are not working all together during a time similar to the one measure on a single optical transmitter, we obtain a similar equivalent bit error rate since we are dominated by single event effect on the Maxim PLL.

In the coming month, we will measure radiation effects on ribbon optical transmitter. Indeed, temperature monitoring of the laser driver is performed by a digital control system based on EEPROM modules. If a single event upsets causes a loss of EEPROM configuration, the optical transmitter could become not operational !

7. Conclusion

To design a high speed optical link, we have chosen a set of components that guaranties, in the worst case, a bit error rate lower than 10^{-12}.

To check the robustness of our conception against various perturbations, we have built a test bench setup to characterize high speed optical links.

The results of measurements are the following :

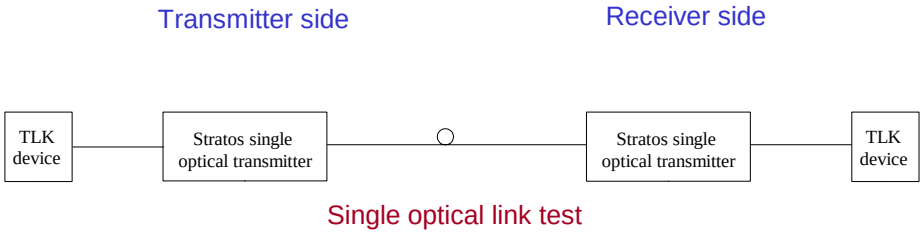
- We are able to transport data with a bit error rate of about 10^{-15} in lab conditions using a low clock jitter ;
- Our design is quite insensitive to power supply variations ;
- The design is very sensitive to the input clock jitter ;
- The level of clock jitter of the TTCrx is not acceptable for a reliable transfer of data (bit error rate is around 10^{-3}) ;
- A jitter filtering solution allowing to use the TTCrx clock has successfully been tested. It allows to obtain a bit error rate around 10^{-15}.
- In the muon environment, we estimate the bit error rate due to the single event upsets to be less than 3.3×10^{-11}

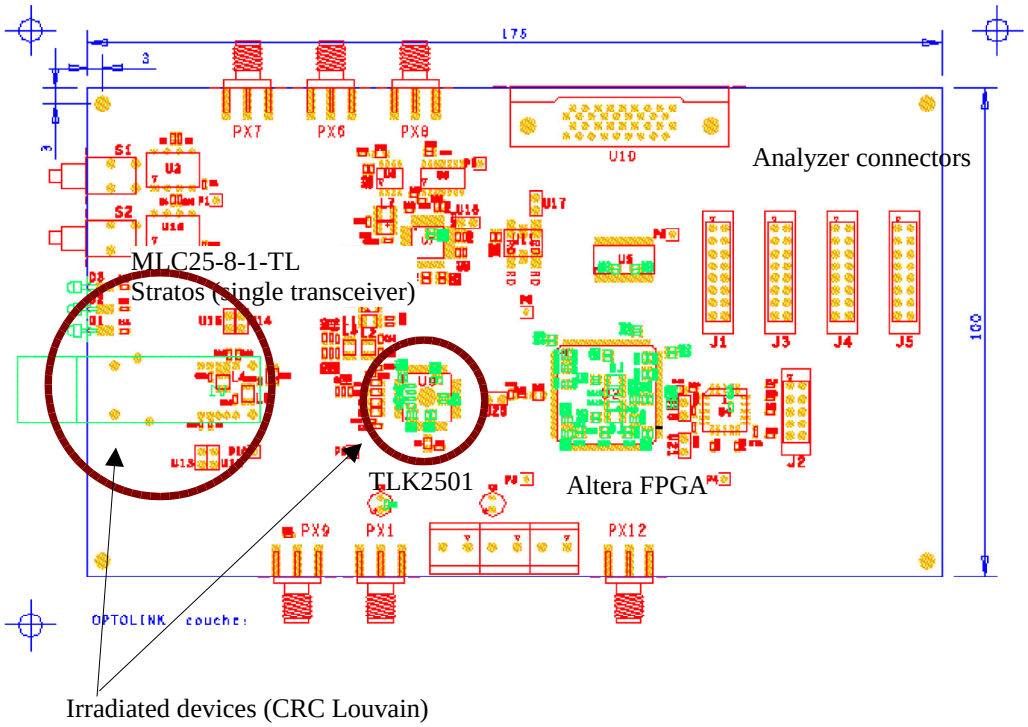
We are now confident that this design will provide a reliable data transfer between the ODE and the muon trigger processor.

In the coming months, we will build an emission board with 24 optical links. It will contain the emission part of the ODE board and will drive two ribbon optical transmitters. Seriliazers will be the GOL chip as well as TLK2501. To filter the TTC jitter we will implement the circuit based on the Maxim chip and the QPLL components. This board will be irradiated to measure the effect of the single event upsets and single event latch up on the ribbon transmitter.

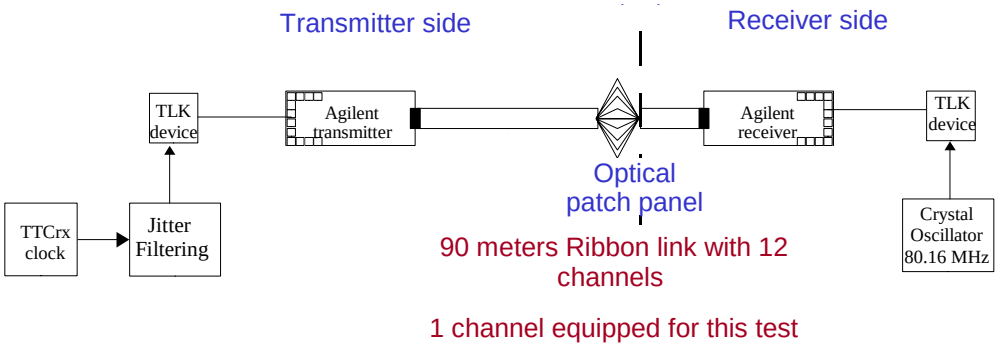
Appendix A : Prototype boards designed for test and characterization

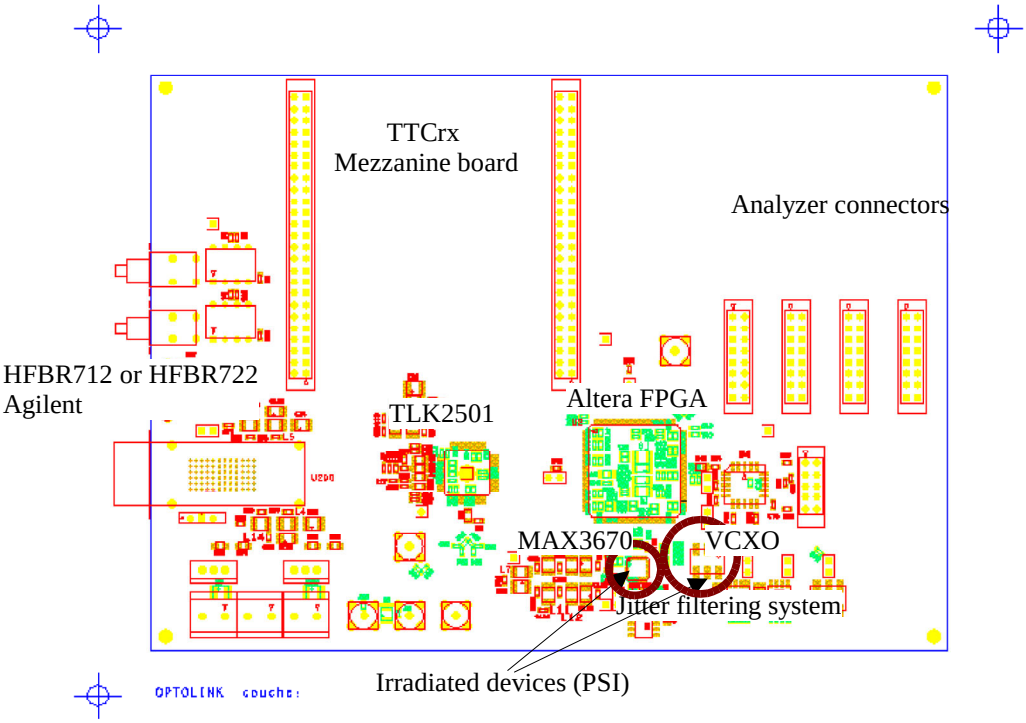
The first version “Optolink1” uses the TLK2501 and the single optical transceiver from StratosLightwave. This board can be programmed in transmitter mode or receiver mode.





The second version “Optolink2” based on the TLK2501 for serialization and deserialization and on the Agilent optical ribbon transmitter and receiver. In that set-up only one channel was equipped over the twelve.





Appendix B : The cost of the ribbon optical link

The price of a 12 way ribbon optical link can be derived from the prototypes we built in 2001 and 2002 :

	Designation	Cost of the Prototype (kCHF)		Predicted Cost (kCHF)	
Serializer	TLK2501 TI	0.576	*EBV quotation for 1-10 pieces*	0.379 (GOL)	*EBV quotation for 500 pieces*
Optical Transmitter	Tx : HFBR712 Agillent	1.312	*EBV quotation for 1 piece*	0.854	*Agilent Web site + a margin of 20%*
Optical Ribbon	Tyco Electonic	1.54	*Source : Tyco France*	1.54	*Source : Tyco France*
Optical Receiver	Rx : HFBR722 Agillent	1.312	*EBV quotation for 1 piece*	0.854	*Agilent Web site + a margin of 20%*
Deseriaizer	TLK2501 TI	0.576	*EBV quotation for 1-10 pieces*	0.402	*EBV quotation for 500 pieces*
PLL + VCXO	Maxim CTS-Corp	0.200	*CTS Quotation for 100 pieces + estimation for maxim chip*	0.200	*CTS Quotation for 100 pieces + estimation for maxim chip*
Crystal Oscillator	Pletronics	0.035	*Source: Compotron 1-10 pieces*	0.035	*Source: Compotron 1-10 pieces*
Cost of 12 optical links		**5.55**		**4.26**	
Cost/1.6 Gbit link		**0.46**		**0.36**	

(December 2002)

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